WHAT IS CLAIMED IS:

1. A packet communication apparatus for processing consecutive fixed-length packets, said apparatus comprising:

a storage circuit;

a first processing circuit which accesses said storage circuit for executing first processing with respect to data obtained from each of said packets;

a second processing circuit which accesses said storage circuit for executing second processing with respect to data stored in said storage circuit; and

an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of said packets, said allocation circuit allocating a first time of said packet processing time to said first processing circuit for accessing said storage circuit and a second time of said packet processing time to said second processing circuit for accessing said storage circuit, said first time and said second time prevented from overlapping with each other.

2. The packet communication apparatus according to claim 1, wherein said storage circuit is a DRAM, and said second processing circuit refreshes said DRAM during said second time.

3. The packet communication apparatus according to claim 1, further comprising a producing circuit which receives a first packet synchronizing signal having first signal components each indicative of a boundary time point between the adjacent packets and produces a second packet synchronizing

signal based on said first packet synchronizing signal, wherein said producing circuit, in response to one of said first signal components, produces in sequence second signal components of said second packet synchronizing signal at a given cycle corresponding to said packet processing time, said given cycle being free of an influence of said first signal components subsequent to said one of said first signal components, and wherein said allocation circuit executes said access time allocation based on said second packet synchronizing signal.

4. The packet communication apparatus according to claim 3, wherein said producing circuit comprises a counter which produces in sequence said second signal components at said given cycle in response to said one of said first signal components, and a control circuit which inhibits any of said first signal components being asynchronous with said given cycle from being inputted into said counter.

5. The packet communication apparatus according to claim 1, further comprising a producing circuit which receives a first packet synchronizing signal having first signal components each indicative of a boundary time point between the adjacent packets and produces a second packet synchronizing signal based on said first packet synchronizing signal, wherein said producing circuit produces second signal components of said second packet synchronizing signal in response to said first signal components such that any of said first signal components which is advanced in phase relative to said packet processing time is prevented from reflecting on said second packet synchronizing signal, and wherein said allocation circuit executes said access time allocation based on said second packet synchronizing signal.

6. The packet communication apparatus according to claim 5, wherein said producing circuit comprises a control circuit which receives said first signal components, and a first counter which produces each of said second signal components in response to a corresponding input from said control circuit, and wherein said control circuit inhibits any of said first signal components, which is advanced in phase relative to said packet processing time, from being inputted into said first counter.

7. The packet communication apparatus according to claim 6, wherein said producing circuit further comprises a second counter which, in response to an input of each of said first signal components, outputs a corresponding signal component to said control circuit, while said second counter outputs a signal component to said control circuit at a given cycle corresponding to said packet processing time when no input is given to said second counter.

8. A packet communication apparatus for processing consecutive fixed-length packets, said apparatus comprising:

a DRAM;

a processing circuit which accesses said DRAM for processing data obtained from each of said packets;

a refresh circuit for refreshing said DRAM; and

an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of said packets, said allocation circuit allocating a first time of said packet processing time to said processing circuit for accessing said DRAM and a second time of said packet processing time to said refresh circuit for refreshing said DRAM, said first time and said second time prevented from overlapping with each other.